

CLAIMS

- 1 1. An apparatus for providing a signal with an adjustable delay, comprising:
2 a delay line, having an input adapted to receive the signal, and including a
3 plurality of taps outputting delayed versions of the signal;
4 a plurality of first stage multiplexers, the first stage multiplexers having inputs
5 coupled to taps in the plurality of taps, and respectively providing signals from taps in the
6 plurality of taps at respective first stage outputs selected in response to first stage control
7 signals;
8 a second stage multiplexer having inputs coupled to the first stage outputs from
9 the plurality of first stage multiplexers, and providing a signal from a selected tap at a
10 second stage output in response to second stage control signals; and
11 logic generating the first and second stage control signals to select one of said
12 plurality of taps as the selected tap, including, for all pairs of adjacent taps in the plurality
13 of taps, logic to change the selected tap to the adjacent tap in the pair by switching only
14 one of the first stage multiplexer or the second stage multiplexer.
- 1 2. The apparatus of claim 1, wherein the signal comprises a clock signal, and the
2 delayed versions of the signal comprise phase shifted versions of the clock signal.
- 1 3. The apparatus of claim 1, wherein said delayed versions of the signal provided
2 from adjacent taps differ in delay by less than 500 picoseconds.
- 1 4. The apparatus of claim 1, wherein said delayed versions of the signal provided
2 from adjacent taps differ in delay by less than 200 picoseconds.
- 1 5. The apparatus of claim 1, wherein said delayed versions of the signal provided
2 from adjacent taps differ in delay by an amount on the order of 100 picoseconds.
- 1 6. The apparatus of claim 1, wherein the signal comprises a clock signal having a
2 frequency greater than 300 MHz, and the delayed versions of the signal comprises phase

3 shifted versions of the clock signal, and the phase shifted versions of the clock signal
4 differ in phase by less than 200 picoseconds.

1 7. The apparatus of claim 1, wherein the delay line comprises a plurality of inverters
2 in series, and the plurality of taps comprise buffers coupled to outputs of inverters in the
3 plurality of inverters.

1 8. The apparatus of claim 1, wherein the logic comprises a first shift register and a
2 second shift register, the output of the first shift register supplying the first control signals
3 and the output of the second shift register supplying the second control signals.

1 9. The apparatus of claim 1, wherein the logic comprises a first bidirectional shift
2 register and a second bidirectional shift register, the output of the first bidirectional shift
3 register supplying the first control signals, the first control signals including a set of
4 unselect bits and a select bit stored in the first bidirectional shift register corresponding
5 with respective inputs of the first stage multiplexers, and the output of the second
6 bidirectional shift register supplying the second control signals, the second control signals
7 including a set of unselect bits and a select bit stored in the second bidirectional shift
8 register corresponding with respective inputs of the second stage multiplexer; and
9 logic to shift unselect bits into the first bidirectional shift register from first and
10 second directions to move the select bit for the first control signals, and to shift unselect
11 bits into the second bidirectional shift register from first and second directions to move
12 the select bit for the second control signals.

1 10. The apparatus of claim 1, wherein the logic comprises a first bidirectional shift
2 register and a second bidirectional shift register, the output of the first bidirectional shift
3 register supplying the first control signals, the first control signals including a set of
4 unselect bits and a select bit stored in the first bidirectional shift register corresponding
5 with respective inputs of the first stage multiplexers, and the output of the second
6 bidirectional shift register supplying the second control signals, the second control signals

7 including a set of unselect bits and a select bit stored in the second bidirectional shift
8 register corresponding with respective inputs of the second stage multiplexer; and
9 logic to shift unselect bits into the first bidirectional shift register from first and
10 second directions to move the select bit for the first control signals, and to shift unselect
11 bits into the second bidirectional shift register from first and second directions to move
12 the select bit for the second control signals, including
13 when the select bit in the second control signals is in even positions in the second
14 bidirectional shift register, shifting the unselect signals into the first bidirectional shift
15 register from the same direction of the one of the first and second directions in which the
16 unselect signals are shifted into the second bidirectional shift register, and when the select
17 bit in the second control signals is in odd positions in the second bidirectional shift
18 register, shifting the unselect signals into the first bidirectional shift register from the
19 opposite direction of the one of the first and second directions in which the unselect
20 signals are shifted into the second bidirectional shift register.

1 11. An apparatus for providing an output signal and an output clock signal with an
2 adjustable phase, comprising:
3 a delay line, having an input adapted to receive a clock signal, and including a
4 plurality of taps outputting phase shifted versions of the clock signal;
5 a plurality of first stage multiplexers, the first stage multiplexers having inputs
6 coupled to taps in the plurality of taps, and respectively providing phase shifted versions
7 of the clock signal from taps in the plurality of taps at respective first stage outputs
8 selected in response to first stage control signals;
9 a second stage multiplexer having inputs coupled to the first stage outputs from
10 the plurality of first stage multiplexers, and providing a selected phase shifted version of
11 the clock signal from a selected tap at a second stage output in response to second stage
12 control signals, as the output clock signal;
13 multiplexer logic generating the first and second stage control signals to select
14 one of said plurality of taps as the selected tap in response to clock control signals,
15 including, for all pairs of adjacent taps in the plurality of taps, logic to change the

16 selected tap to the adjacent tap in the pair by switching either the first stage multiplexers
17 or the second stage multiplexer, but not both; and
18 logic to generate the clock control signals in response to relative timing of the
19 output signal and the output clock signal.

1 12. The apparatus of claim 11, including:
2 a memory including memory cells, and having address/data paths and timing
3 paths which emulate the address/data paths, the address/data paths outputting said output
4 signal in response to addresses; and
5 an output clock phase detector coupled to the logic to generate the clock control
6 signals and to the memory, which generates signals indicating the relative phase of
7 transitions of the output signal and the output clock signal.

1 13. The apparatus of claim 11, including:
2 a memory including memory cells, and having address/data paths and timing
3 paths which emulate the address/data paths, the address/data paths outputting data in
4 response to addresses and the timing paths outputting dummy data in response to an
5 address emulation signal;
6 an output clock phase detector coupled to the logic to generate the clock control
7 signals and to the memory, which generates signals indicating the relative phase of
8 transitions of the output signal and the output clock signal; and
9 delay locked loop, responsive to an input clock, to generate an address emulation
10 signal on the timing paths in the memory.

1 14. The apparatus of claim 11, wherein said phase shifted versions of the clock signal
2 provided from adjacent taps differ in phase by less than 500 picoseconds.

1 15. The apparatus of claim 11, wherein said phase shifted versions of the clock signal
2 provided from adjacent taps differ in phase by less than 200 picoseconds.

1 16. The apparatus of claim 11, wherein said phase shifted versions of the clock signal
2 provided from adjacent taps differ in phase by an amount on the order of 100
3 picoseconds.

1 17. The apparatus of claim 11, wherein the clock signal has a frequency greater than
2 300 MHz, and the phase shifted versions of the clock signal provided from adjacent taps
3 differ in phase by less than 200 picoseconds.

1 18. The apparatus of claim 11, wherein the delay line comprises a plurality of
2 inverters in series, and the plurality of taps comprise buffers coupled to outputs of
3 inverters in the plurality of inverters.

1 19. The apparatus of claim 11, wherein the multiplexer logic comprises a first shift
2 register and a second shift register, the output of the first shift register supplying the first
3 control signals and the output of the second shift register supplying the second control
4 signals.

1 20. The apparatus of claim 11, wherein the multiplexer logic comprises a first
2 bidirectional shift register and a second bidirectional shift register,
3 the output of the first bidirectional shift register supplying the first control signals,
4 the first control signals including a set of unselect bits and a select bit stored in the first
5 bidirectional shift register corresponding with respective inputs of the first stage
6 multiplexers, and
7 the output of the second bidirectional shift register supplying the second control
8 signals, the second control signals including a set of unselect bits and a select bit stored in
9 the second bidirectional shift register corresponding with respective inputs of the second
10 stage multiplexer; with
11 logic to shift unselect bits into the first bidirectional shift register from first and
12 second directions to move the select bit for the first control signals, and to shift unselect
13 bits into the second bidirectional shift register from first and second directions to move
14 the select bit for the second control signals.

1 21. The apparatus of claim 11, wherein the multiplexer logic comprises a first
2 bidirectional shift register and a second bidirectional shift register,
3 the output of the first bidirectional shift register supplying the first control signals,
4 the first control signals including a set of unselect bits and a select bit stored in the first
5 bidirectional shift register corresponding with respective inputs of the first stage
6 multiplexers, and
7 the output of the second bidirectional shift register supplying the second control
8 signals, the second control signals including a set of unselect bits and a select bit stored in
9 the second bidirectional shift register corresponding with respective inputs of the second
10 stage multiplexer; with
11 logic to shift unselect bits into the first bidirectional shift register from first and
12 second directions to move the select bit for the first control signals, and to shift unselect
13 bits into the second bidirectional shift register from first and second directions to move
14 the select bit for the second control signals, including
15 when the select bit in the second control signals is in even positions in the second
16 bidirectional shift register, shifting the unselect signals into the first bidirectional shift
17 register from the same direction of the one of the first and second directions in which the
18 unselect signals are shifted into the second bidirectional shift register, and
19 when the select bit in the second control signals is in odd positions in the second
20 bidirectional shift register, shifting the unselect signals into the first bidirectional shift
21 register from the opposite direction of the one of the first and second directions in which
22 the unselect signals are shifted into the second bidirectional shift register.

1 22. A method for selecting an output of a delay line comprising a plurality of taps, the
2 plurality of taps including a plurality of sets of taps, comprising:
3 selecting in a first stage, selected taps from respective sets in the plurality of sets
4 of taps;
5 selecting in a second stage, an output tap from the selected taps from the first
6 stage; and

- 7 controlling the selecting in first stage and the selecting in the second stage
- 8 selecting, for all pairs of adjacent taps in the plurality of taps, to change the output tap to
- 9 the adjacent tap in the pair by switching in only one of the first stage or the second stage.